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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,828	05/27/2005	Makoto Kitabatake	071971-0251	6640

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MCDERMOTT WILL & EMERY LLP
600 13TH STREET, N.W.
WASHINGTON, DC 20005-3096

EXAMINER	
KALAM, ABUL	
ART UNIT	PAPER NUMBER
2814	

MAIL DATE	DELIVERY MODE
12/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,828	KITABATAKE ET AL.	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 12-19* is/are pending in the application.

4a) Of the above claim(s) *5,6 and 12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/22/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 12, 2008, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. **Claims 1, 2, 15 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Teshima et al. (US 2003/0132530)** in view of **Litwin (US 6,507,047)**.

With respect to **claim 1, Teshima** teaches a semiconductor apparatus **(Fig. 3)** comprising:

a semiconductor chip **(1, Fig. 3)** including a power semiconductor device **(¶ [0033]: "IGBT chip")**;

a first base material **(5, Fig. 3)** made of an electrically conductive material **(¶ [0037]: copper alloy)** and electrically connected **(through solder 4)** to a part of a lower surface **(1b)** of said semiconductor chip **(1)**;

a heat conducting member **(3/4, Fig. 3)** coming in contact with a part of an upper surface **(1a)** of said semiconductor chip and releasing heat directly from said semiconductor chip **(¶ [0040])**;

an encapsulating material **(9, Fig. 3)** for encapsulating said semiconductor chip **(1)** and said heat conducting member **(3/4)**;

wherein the semiconductor apparatus further comprises a second base material **(7, Fig. 3)** made of a metal material and connected to a part of said upper surface **(1a)** of said semiconductor chip **(1)**,

wherein said power semiconductor device is a vertical element **(¶ [0033])**,

wherein a part of said first base material **(5, Fig. 3)** is extruded outside said encapsulating material **(9)** and works as a first external connection terminal **(¶ [0037]-[0038])**;

wherein a part of said second base material **(7, Fig. 3)** is extruded outside said encapsulating material **(9)** and works as a second external connection terminal **(¶ [0038])**,

wherein a first intermediate member **(4, Fig. 3)** made of an electrically conductive material **(¶ [0037]: solder)** and a second intermediate member **(15, ¶ [0032], [0048])**

made of a material **(¶ [0048]: resin)** having lower heat conductivity than said first intermediate member **(solder 4)** are provided between said first base material **(5)** and said semiconductor chip **(1)**; and

wherein the semiconductor chip **(1, Fig. 3)** and the first base material **(5)** are electrically connected with each other through the first intermediate member **(4, ¶ [0037])**.

Thus, **Teshima** teaches all the limitations of the claim with the exception of disclosing: a wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material **(SiC) (col. 1: lns. 35-67)**. **Litwin** discloses that transistors based on silicon carbide, which is a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Teshima** to include wide band gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips **(col. 2: lns. 1-10)**.

With respect to **claim 2, Teshima and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, "wherein said power semiconductor device has a region where a current passes at a current density of 50

A/cm^2 or more," Applicant has not shown such a claimed range to be critical or yield unpredictable results, and thus, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form a power semiconductor device with a current density as claimed, because the prior art teaches a device substantially identical in structure and material, to that of Applicant's claimed invention.

With respect to **claim 15, Teshima** teaches wherein another heat conducting member **(314, Fig. 9)** is in direct contact with the lower face of said semiconductor chip **(301, Fig. 9)**.

With respect to **claim 19, Lin and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Furthermore, **Litwin** teaches wherein said wide band gap semiconductor is SiC **(col. 1: lns. 63-66)**.

3. **Claims 1-4, 16, 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Mamitsu et al. (US 6,703,707)** in view of **Litwin (US '047; cited above)**.

With respect to **claim 1, Mamitsu** teaches a semiconductor apparatus **(Figs. 8A and 8B)** comprising:

a semiconductor chip **(1a, Fig. 8A)** including a power semiconductor device **(col. 5, lns. 5-6)**;

a first base material **(3, Fig. 8A)** made of an electrically conductive material **(col. 5, lns. 46-51)** and electrically connected **(through bond members 4, col. 5, lns. 60-61)** to a part of a lower surface of said semiconductor chip **(1a)**;

a heat conducting member **(2a/4, Fig. 8A)** coming in contact with a part of an upper surface of said semiconductor chip **(1a)** and releasing heat directly from said semiconductor chip **(col. 6, lns. 39-41)**;

an encapsulating material **(9, Fig. 8A)** for encapsulating said semiconductor chip **(1b)** and said heat conducting member **(2a/4)**;

wherein the semiconductor apparatus further comprises a second base material **(5, Fig. 3; col. 4, ln. 58)** made of a metal material and connected to a part of said upper surface **(1a)** of said semiconductor chip **(1)**,

wherein said power semiconductor device is a vertical element **(col. 5, lns. 36-41)**,

wherein a part of said first base material **(3, Fig. 8A)** is extruded outside said encapsulating material **(9)** and works as a first external connection terminal **(col. 6, lns. 3-4)**;

wherein a part of said second base material **(5, Fig. 8A)** is extruded outside said encapsulating material **(9)** and works as a second external connection terminal **(col. 6, lns. 1-2)**,

wherein a first intermediate member **(4, Fig. 8A)** made of an electrically conductive material **(col. 5, lns. 60-61: solder)** and a second intermediate member **(18, Fig. 8A)** made of a material **(col. 12, ln. 18: resin)** having lower heat conductivity than

said first intermediate member **(solder 4)** are provided between said first base material **(3)** and said semiconductor chip **(1a; col. 12, lns. 51-60)**; and

wherein the semiconductor chip **(1a, Fig. 8A)** and the first base material **(3)** are electrically connected with each other through the first intermediate member **(4)**.

Thus, **Mamitsu** teaches all the limitations of the claim with the exception of disclosing: a wide band gap semiconductor.

However, **Litwin** discloses semiconductor chips containing power transistors constructed by using wide band gap semiconductor material **(SiC) (col. 1: lns. 35-67)**. **Litwin** discloses that transistors based on silicon carbide, which is a well known wide bandgap semiconductor, are another alternative to transistors based on Si or GaAs for power applications at high frequencies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the semiconductor chip of **Mamitsu** to include wide band gap semiconductor devices, as taught by **Litwin**, because semiconductor devices based on silicon carbide (SiC) are capable of handling high power densities and can operate at high temperatures, thus improving the speed, reliability and performance of semiconductor chips **(col. 2: lns. 1-10)**.

With respect to **claim 2, Mamitsu and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Regarding the limitation, "wherein said power semiconductor device has a region where a current passes at a current density of 50 A/cm^2 or more," Applicant has not shown such a claimed range to be critical or yield unpredictable results, and thus, absent evidence of disclosure of criticality for the range

giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. See *In re Aller*, 220 F.2d 454, 105 USPQ 233, 234 (CCPA 1955). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to form a power semiconductor device with a current density as claimed, because the prior art teaches a device substantially identical in structure and material, to that of Applicant's claimed invention.

With respect to **claim 3, Mamitsu** teaches wherein said encapsulating material **(9, Fig. 4)** is made of a resin or glass **(col. 5, lns. 65-67)**, and said heat conducting member **(2a)** is exposed from said encapsulating material **(col. 5, lns. 65-67)**.

With respect to **claim 4, Mamitsu** teaches wherein said apparatus further comprises a radiation fin **(2, Fig. 8A)** that is contact with said heat conducting member **(2a)** and is extruded outside said encapsulating material **(9)**.

With respect to **claim 16, Mamitsu** teaches **(Fig. 8B, col. 12, lns. 51-60)** wherein a contact area between said semiconductor chip **(1a)** and said base material **(3)** is smaller than a half of an area of the upper or lower surface of said semiconductor chip **(1a)**.

With respect to **claim 18, Mamitsu** teaches wherein said external connection terminal of said first base material **(3)** is constructed to be mounted **(col. 6, lns. 2-4: "electrodes")** on a print wiring board. It is well known in the art that electrodes are capable of being mounted on a print wiring board. Furthermore, note that limitation of "constructed to be mounted on a print wiring board," is considered functional language. It has been held that an apparatus must be distinguished from the prior art in terms of

structure rather than function. *In re Schreiber,* 128 F.3d 1473, 1477-78, 44USPQ2d 1429, 1431-32 (Fed. Cir. 1997).

With respect to **claim 19, Mamitsu and Litwin** teach the semiconductor apparatus of claim 1, as set forth above. Furthermore, **Litwin** teaches wherein said wide band gap semiconductor is SiC **(col. 1: lns. 63-66)**.

4. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Teshima et al. (US '530; cited above)** and **Litwin ('047; cited above)**, as applied to claim 3 above, and further in view of **Wu et al. (US 6,590,281).**

With respect to **claim 17, Teshima** further discloses another semiconductor chip **(2, Fig. 3)**, which is also connected to said first base material **(5)**. However, neither **Teshima** nor **Litwin** teach wherein said another semiconductor that is stacked on the first semiconductor chip.

However, **Wu** teaches a semiconductor apparatus wherein a semiconductor chip **(24, Fig. 4)** that is stacked on another semiconductor chip **(25)**. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to combine the teaching of Wu, with the teachings of Teshima and Litwin, to form a semiconductor apparatus wherein two semiconductor chips are stacked on top of each other, for the purpose of reducing the size the package.

Response to Arguments

5. Applicant's arguments filed November 12, 2008, have been considered but are moot in view of new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is (571)272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./
Examiner, Art Unit 2814

/Phat X. Cao/
Primary Examiner, Art Unit 2814